DOCKET NO. 00-C-050 (STMI01-00050)
Customer No. 30425

1251

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	William E. Ballachino
Serial No.	:	09/667,164
Filed	:	September 21, 2000
For	:	M-BIT RACE DELAY ADDER AND METHOD OF OPERATION
Group No.	:	2193
Examiner	:	Chat C. Do

MAIL STOP 16
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REQUEST FOR REFUND

Applicant hereby requests a refund in the amount of $120.00 for the one-month extension fee charged to Munck Butrus Deposit Account No. 50-0208 on January 23, 2008. A copy of the Deposit Account Statement dated January 2008 is attached.

Applicant filed an Amendment and Response to Office Action on December 26, 2007 in response to the Office Action dated September 24, 2007. A copy of the Amendment and Response to Office Action as filed on December 26, 2007, and date-stamped postcard, are enclosed. Since the U.S. Patent and Trademark Office was closed for the Christmas holiday on December 24, 2007 and December 25, 2007, the response due date was extended to December 26, 2007. Therefore, this Amendment was timely filed and no extension fee was required.

Please issue a credit in the amount of $120.00 to Deposit Account No. 50-0208 for this charge.

Respectfully submitted,

MUNCK BUTRUS CARTER, P.C.

Date: March 12, 2008

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United States Patent and Trademark Office

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Deposit Account Statement

Requested Statement Month:	January 2008
Deposit Account Number:	500208
Name:	MUNCK BUTRUS, P.C.
Attention:	JOHN T MOCKLER
Street Address 1:	900 THREE GALLERIA TOWER
Street Address 2:	13155 NOEL ROAD
City:	DALLAS
State:	TX
Zip:	75240
Country:	UNITED STATES

DATE	SEQ	POSTING REF TXT	ATTORNEY DOCKET NBR	FEE CODE	AMT	B/
01/02	852	11496752		8021	$40.00	$5
01/03	84	11827142	10628ROUS07C (NORT10-0056	1201	$750.00	$4
01/03	95	11903508	WEST14-00149	2081	$130.00	$4
01/04	2	11827142	10628ROUS07C (NORT10-0056	1201	-$750.00	$5
01/07	28	11899849	P06915	1251	$120.00	$5
01/08	105	12006850	YPF200704-0089/US(SAMS07-	1202	$50.00	$5
01/08	107	12006850	YPF200704-0089/US(SAMS07-	1203	$370.00	$5
01/09	4648	77057113	SAMS02-00083	7004	$150.00	$4
01/11	2824	78606128	CART05-00004	7004	$150.00	$4
01/11	10954	77369400	SAMS02-00097	7001	$325.00	$4
01/15	1	10606847	BA0346.2C (NORT10-00324)	1251	$120.00	$4
01/17	1346	11982849		8021	$40.00	$4
01/17	4	11035331	P06123	1251	$120.00	$4
01/22	12482	12017092	H0017647-0109	1011	$310.00	$3
01/22	12483	12017092	H0017647-0109	1111	$510.00	$3
01/22	12484	12017092	H0017647-0109	1311	$210.00	$3
01/22	12530	12017092		8021	$40.00	$3
01/22	14226	12017172	H0017492-0109	1011	$310.00	$2
01/22	14228	12017172	H0017492-0109	1311	$210.00	$2
01/22	14227	12017172	H0017492-0109	1111	$510.00	$2
01/22	14229	12017172	H0017492-0109	1202	$50.00	$2
01/22	14319	12017172		8021	$40.00	$1
01/22	15526	E-REPLENISHMENT		9203	-$2,190.00	$4
01/22	2	10836885	2003.10.015.WT0	1251	$120.00	$4
01/22	20259	12017469	H0017381-0109	1011	$310.00	$3
01/22	20262	12017469	H0017381-0109	1202	$50.00	$3

01/22	20260	12017469	H0017381-0109	1111	$510.00	$
01/22	20261	12017469	H0017381-0109	1311	$210.00	$
01/22	20357	12017469		8021	$40.00	$
01/22	20824	12017497	H0017648-0109	1011	$310.00	$
01/22	20826	12017497	H0017648-0109	1311	$210.00	$
01/22	20827	12017497	H0017648-0109	1202	$50.00	$
01/22	20825	12017497	H0017648-0109	1111	$510.00	$
01/22	20921	12017497		8021	$40.00	$
01/23	674	E-REPLENISHMENT		9203	-$2,240.00	$
01/23	3689	77377592	SAMS02-00098	7001	$325.00	$
01/23	1	09667164	00-C-050 (STMI01-00050)	1251	$120.00	$
01/23	13803	12018406	H0012064-0103	1011	$310.00	$
01/23	13804	12018406	H0012064-0103	1111	$510.00	$
01/23	13805	12018406	H0012064-0103	1311	$210.00	$
01/23	13948	12018406		8021	$40.00	$
01/24	4359	E-REPLENISHMENT		9203	-$1,070.00	$
01/28	25	E-REPLENISHMENT		9203	-$3,210.00	$
01/28	1602	12020093	H0017289-0783	1011	$310.00	$
01/28	1603	12020093	H0017289-0783	1111	$510.00	$
01/28	1604	12020093	H0017289-0783	1311	$210.00	$
01/28	1793	12020093		8021	$40.00	$
01/28	2620	12020180	H0017286-0783	1011	$310.00	$
01/28	2622	12020180	H0017286-0783	1311	$210.00	$
01/28	2621	12020180	H0017286-0783	1111	$510.00	$
01/28	2797	12020180		8021	$40.00	$
01/28	3417	12020227	H0017290-0783	1011	$310.00	$
01/28	3419	12020227	H0017290-0783	1311	$210.00	$
01/28	3418	12020227	H0017290-0783	1111	$510.00	$
01/28	3676	12020227		8021	$40.00	$
01/28	6090	E-REPLENISHMENT		9203	-$3,204.00	$
01/29	3803	77382432	KIDK01-00052	7001	$325.00	$
01/29	3835	77382437	KIDK01-00053	7001	$325.00	$
01/29	5697	2131955	SYNC01-00012	7205	$100.00	$
01/29	5698	2131955	SYNC01-00012	7201	$400.00	$

START BALANCE	SUM OF CHARGES	SUM OF REPLENISH	END BALANCE
$5,787.00	$12,790.00	$12,664.00	$5,661.00

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Mailed:	December 26, 2007
In re: Application of:	William E. Ballachino
Application No.:	09/667,164
Filed:	September 21, 2000
Title:	M-BIT RACE DELAY ADDER AND METHOD OF OPERATION
Docket No.:	00-C-050
Client No.:	STMI01-00050

The following documents were received in the U.S. Patent and Trademark Office on the date stamped below:

1) Certificate of Mailing by First Class Mail; and
2) Amendment and Response to Office Action.

DOCKET NO. 00-C-050 (STMI01-00050) PATENT
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	William E. Ballachino
Serial No.	:	09/667,164
Filed	:	September 21, 2000
For	:	M-BIT RACE DELAY ADDER AND METHOD OF OPERATION
Group No.	:	2193
Examiner	:	Chat C. Do

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

Sir:

The undersigned hereby certifies that the following documents:

1. Amendment and Response to Office Action; and
2. A postcard receipt;

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 26, 2007.

Date: 12/26/07 Kathy Ceder
Mailer

Date: 12/26/2007 Robert D. McCutcheon
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DOCKET NO. 00-C-050 (STMI01-00050) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	William E. Ballachino
Serial No.	:	09/667,164
Filed	:	September 21, 2000
For	:	M-BIT RACE DELAY ADDER AND METHOD OF OPERATION
Group No.	:	2193
Examiner	:	Chat C. Do

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

AMENDMENT AND RESPONSE TO OFFICE ACTION

No fees are believed to be necessary; however, in the event that any fees are required for the prosecution of this application, please charge any necessary fees to Deposit Account No. 50-0208. No extension of time is believed to be necessary. If, however, an extension of time is needed, the extension is requested and please charge the fee for this extension to Deposit Account No. 50-0208.

In response to the Office Action having a mailing date of September 24, 2007, please amend the above-identified application as follows:

AMENDMENTS TO THE CLAIMS:

1. (Previously Presented) An M-bit adder capable of receiving a first M-bit argument, a second M-bit argument, and a carry-in (CI) bit comprising:

M adder cells arranged in R rows, wherein a least significant adder cell in a first one of said rows of adder cells is operable to:

receive a first data bit, A_X, from said first M-bit argument and a first data bit, B_X, from said second M-bit argument,

generate both a first conditional carry-out bit, $C_X(1)$, and a second conditional carry-out bit, $C_X(0)$,

provide the first and second conditional carry-out bits $C_X(1)$ and $C_X(0)$ to a second one of said adder cells, and

wherein said $C_X(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells preceding said first row is a 1 and said $C_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0; and

wherein said second one of said adder cells in said first one of said rows is operable to:

receive a first data bit, A_{X+1}, from said first M-bit argument and a first data bit, B_{X+1}, from said second M-bit argument,

receive both said first conditional carry-out bit, $C_X(1)$ and said second conditional carry-out bit, $C_X(0)$;

generate both a first conditional carry-out bit, $C_{X+1}(1)$, and a second conditional carry-out bit, $C_{X+1}(0)$ by propagating said first conditional carry-out bit, $C_X(1)$ and said second conditional carry-out bit, $C_X(0)$ through a first pass gate and a second pass gate, respectively, when said first data bit A_{X+1} and said second data bit B_{X+1} are not equal, and

output said first and second conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$ to other circuitry.

2. (Original) The M-bit adder as set forth in Claim 1 wherein said least significant adder cell generates a first conditional sum bit, $S_X(1)$, and a second conditional sum bit, $S_X(0)$.

3. (Original) The M-bit adder as set forth in Claim 2 wherein said $S_X(1)$ bit is calculated assuming said row carry-out bit from said second row is a 1 and said $S_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

4. (Original) The M-bit adder as set forth in Claim 3 wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said least significant adder cell.

5. (Previously Presented) The M-bit adder as set forth in Claim 4 wherein said other circuitry comprises:

a third adder cell in said first one of said rows of adder cells, and wherein said third adder cell receives a third data bit, A_{X+2}, from said first M-bit argument and a third data bit, B_{X+2}, from said second M-bit argument, and receives from said second adder cell said $C_{X+1}(1)$ bit and said $C_{X+1}(0)$ bit.

6. - 7. (Canceled).

8. (Previously Presented) The M-bit adder as set forth in Claim 4 wherein said second adder cell generates a first conditional sum bit, $S_{X+1}(1)$, wherein said $S_{X+1}(1)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(1)$ bit from said least significant adder cell.

9. (Original) The M-bit adder as set forth in Claim 8 wherein said second adder cell generates a second conditional sum bit, $S_{X+1}(0)$, wherein said $S_{X+1}(0)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(0)$ bit from said least significant adder cell.

10. (Original) The M-bit adder as set forth in Claim 9 wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

11. (Original) The M-bit adder as set forth in Claim 1 wherein said first row of adder cells contains N adder cells and said second row of adder cells preceding said first row contains less than N adder cells.

12. (Previously Presented) A data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline, wherein at least one of said N processing stages comprises an M-bit adder capable of receiving a first M-bit argument, a second M-bit argument, and a carry-in (CI) bit, said M-bit adder comprising:

M adder cells arranged in R rows, wherein a least significant adder cell in a first one of said rows of adder cells is operable to:

receive a first data bit, A_X, from said first M-bit argument and a first data bit, B_X, from said second M-bit argument,

generate both a first conditional carry-out bit, $C_X(1)$, and a second conditional carry-out bit, $C_X(0)$,

provide the first and second conditional carry-out bits $C_X(1)$ and $C_X(0)$ to a second one of said adder cells, and

wherein said $C_X(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells preceding said first row is a 1 and said $C_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0; and

wherein said second one of said adder cells in said first one of said rows is operable to:

receive a first data bit, A_{X+1}, from said first M-bit argument and a first data bit, B_{X+1}, from said second M-bit argument,

receive both said first conditional carry-out bit, $C_X(1)$ and said second conditional carry-out bit, $C_X(0)$;

generate both a first conditional carry-out bit, $C_{X+1}(1)$, and a second conditional carry-out bit, $C_{X+1}(0)$ by propagating said first conditional carry-out bit, $C_X(1)$ and said second conditional carry-out bit, $C_X(0)$ through a first pass gate and a second pass gate, respectively, when said first data bit A_{X+1} and said second data bit B_{X+1} are not equal, and

output said first and second conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$..

13. (Original) The data processor as set forth in Claim 12 wherein said least significant adder cell generates a first conditional sum bit, $S_X(1)$, and a second conditional sum bit, $S_X(0)$.

14. (Original) The data processor as set forth in Claim 13 wherein said $S_X(1)$ bit is calculated assuming said row carry-out bit from said second row is a 1 and said $S_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

15. (Original) The data processor as set forth in Claim 14 wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said least significant adder cell.

16. (Previously Presented) The data processor as set forth in Claim 15 wherein said other circuitry comprises:

a third adder cell in said first one of said rows of adder cells, and wherein said third adder cell receives a third data bit, A_{X+2}, from said first M-bit argument and a third data bit, B_{X+2}, from said second M-bit argument, and receives from said second adder cell said $C_{X+1}(1)$ bit and said $C_{X+1}(0)$ bit.

17. - 18. (Canceled).

19. (Previously Presented) The data processor as set forth in Claim 15 wherein said second adder cell generates a first conditional sum bit, $S_{X+1}(1)$, wherein said $S_{X+1}(1)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(1)$ bit from said least significant adder cell.

20. (Original) The data processor as set forth in Claim 19 wherein said second adder cell generates a second conditional sum bit, $S_{X+1}(0)$, wherein said $S_{X+1}(0)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(0)$ bit from said least significant adder cell.

21. (Original) The data processor as set forth in Claim 20 wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

22. (Original) The data processor as set forth in Claim 12 wherein said first row of adder cells contains N adder cells and said second row of adder cells preceding said first row contains less than N adder cells.

23. (Previously Presented) A method of adding a first M-bit argument and a second M-bit argument in an M-bit adder, the M-bit adder comprising M adder cells arranged in R rows, the method comprising the steps of:

receiving a first data bit, A_X, from the first M-bit argument and a first data bit, B_X, from the second M-bit argument in a least significant adder cell in a first one of the rows of adder cells;

calculating in the least significant adder cell a first conditional carry-out bit, $C_X(1)$, assuming a row carry-out bit from a second row of adder cells preceding the first row is a 1;

calculating in the least significant adder cell a second conditional carry-out bit, $C_X(0)$, assuming the row carry-out bit from the second row is a 0;

calculating in the least significant adder cell a first conditional sum bit, $S_X(1)$, assuming the row carry-out bit from the second row is a 1;

calculating in the least significant adder cell a second conditional sum bit, $S_X(0)$, assuming the row carry-out bit from the second row is a 0;

propagating the $C_X(1)$ bit and the $C_X(0)$ bit to a second adder cell in the first row of adder cells;

selecting one of the $S_X(1)$ bit and the $S_X(0)$ bit to be output from the least significant adder cell according to a value of the row carry-out bit from the second row; and.

receiving a first data bit, A_{X+1}, from the first M-bit argument and a first data bit, B_{X+1}, from the second M-bit argument in the second adder cell in said first one of said rows of adder cells;

generating in said second adder cell both a first conditional carry-out bit, $C_{X+1}(1)$, and a second conditional carry-out bit, $C_{X+1}(0)$ by propagating said first conditional carry-out bit $C_X(1)$ and said second conditional carry-out bit $C_X(0)$ through a first pass gate and a second pass gate, respectively, when said first data bit A_{X+1} and said second data bit B_{X+1} are not equal, and

outputting said first and second conditional carry-out bits $C_{X+1}(1)$ and $C_{X+1}(0)$ to other circuitry.

24. (Previously Presented) The M-bit adder as set forth in Claim 1 wherein said second adder cell further comprises:

a first inverter operable for inverting said first conditional carry-out bit $C_X(1)$ transmitted through said first pass gate prior to outputting said first conditional carry-out bit $C_X(1)$; and

a second inverter operable for inverting said second conditional carry-out bit $C_X(0)$ transmitted through said second pass gate prior to outputting said second conditional carry-out bit $C_X(0)$.

25. (Previously Presented) The M-bit adder as set forth in Claim 1 wherein said second adder cell further comprises:

a first inverter operable for inverting said received conditional carry-out bit $C_X(1)$ prior to transmission through said first pass gate; and

a second inverter operable for inverting said received second conditional carry-out bit $C_X(0)$ prior to transmission through said second pass gate.

26. (Previously Presented) The M-bit adder as set forth in Claim 1 wherein said other circuitry comprises:

a row multiplexer, wherein said row carry-out bit from said second row of adder cells preceding said first row selects one of said $C_{X+1}(1)$ bit and said $C_{X+1}(0)$ bit to be output by said row multiplexer.

27. (Previously Presented) The M-bit adder as set forth in Claim 9 wherein said first adder cell comprises:

a first multiplexer operable for receiving said first conditional sum bit, $S_X(1)$ and said second conditional sum bit $S_X(0)$, wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said first adder cell; and

said second adder cell comprises:

a second multiplexer operable for receiving said second conditional sum bit $S_{X+1}(1)$ and said second conditional sum bit $S_{X+1}(0)$, wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

28. (Previously Presented) The data processor as set forth in Claim 12 wherein said second adder cell further comprises:

a first inverter operable for inverting said first conditional carry-out bit $C_X(1)$ transmitted through said first pass gate prior to outputting said first conditional carry-out bit $C_X(1)$; and

a second inverter operable for inverting said second conditional carry-out bit $C_X(0)$ transmitted through said second pass gate prior to outputting said second conditional carry-out bit $C_X(0)$.

29. (Previously Presented) The data processor as set forth in Claim 12 wherein said second adder cell further comprises:

a first inverter operable for inverting said received conditional carry-out bit $C_X(1)$ prior to transmission through said first pass gate; and

a second inverter operable for inverting said received second conditional carry-out bit $C_X(0)$ prior to transmission through said second pass gate.

30. (Previously Presented) The data processor as set forth in Claim 12 wherein said other circuitry comprises:

a row multiplexer, wherein said row carry-out bit from said second row of adder cells preceding said first row selects one of said $C_{X-1}(1)$ bit and said $C_{X+1}(0)$ bit to be output by said row multiplexer.

31. (Previously Presented) The data processor as set forth in Claim 20 wherein said first adder cell comprises:

a first multiplexer operable for receiving said first conditional sum bit, $S_X(1)$ and said second conditional sum bit $S_X(0)$, wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said first adder cell; and

said second adder cell comprises:

a second multiplexer operable for receiving said second conditional sum bit $S_{X+1}(1)$ and said second conditional sum bit $S_{X+1}(0)$, wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

REMARKS

Claims 1-5, 8-16 and 19-31 are pending in the application.

Claims 1-5, 8-16 and 19-31 have been rejected.

No Claims have been amended, and reconsideration is respectfully requested in light of the arguments set forth below.

I. REJECTION UNDER 35 U.S.C. § 101

Claims 1-5, 8-16 and 19-31 are newly rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. The rejection is respectfully traversed.

The Office Action asserts these claims "merely disclose steps/components for adding two arguments without further disclosing a practical/physical application or a useful and tangible result since the claims appear to preempt every substantial practical application of the idea embodied by the claim . . ". Office Action, page 2. This rejection and the underlying reasoning are not well taken for the reasons set forth below.

Independent Claim 1 recites an apparatus. The apparatus clearly defines structure (M adder cells arranged in M rows) operable for performing various functions to produce some concrete and tangible result. These functions include generating at least four conditional carry-out bits, propagating certain carryout bits through pass gates (first pass gate, second pass gate), and outputting two conditional carryout bits to other circuitry. Section 101 clearly contemplates this apparatus or machine as statutory subject matter.

Independent Claim 12 recites a data processor. The data processor clearly defines structure (an instruction pipeline having N stages, at least one stage having an M-bit adder with M adder cells arranges in R rows) operable for performing various functions to produce some concrete and tangible result. These same functions are described in the preceding paragraph. Similarly, section 101 clearly contemplates this structure meeting the statutory requirement.

Independent Claim 23 recites a method (process). Section 101 defines a process as statutory subject matter. The method includes receiving data bits, calculating carryout bits, selecting one bit out of two bits, generating carryout bits, and outputting carryout bits to other circuitry. This method unambiguously produces some concrete and tangible result using a specific method.

Accordingly, Applicant's claims fall within statutory subject matter, and the Applicant respectfully requests withdrawal of the § 101 rejection of Claims 1-5, 8-16 and 19-31.

II. REJECTION UNDER 35 U.S.C. § 102

Claims 1-5, 8-16 and 19-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Uya (US 4,682,303). The rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is

found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

In reply to Applicant's prior response, the Office Action now clarifies that the adder cells in Uya that may be the least significant bit adders cells in a row of adder cells may be either the Bit 0, Bit 4, Bit 8, Bit 13, or Bit 19 adder cell. First, Applicant's claims recite that its least significant adder cell receives first and second conditional carryout bits. Since Uya's Bit 0 adder cell does not receive any conditional carryout bits, the Bit 0 adder cannot meet this limitation. Second, Applicant's claims recite that the conditional carryout bits generated by the least significant bit adder of the first row are calculated assuming row carry-out bits of 0 and 1 from a second row of adders preceding the first row. Since Uya's Bit 4 adder cell does not receive any conditional carryout bits from the P1 adder, Uya's Bit 4 adder cell does not meet this limitation. This only leaves Uya's Bit 8, Bit 13 or Bit 19 adder cells which might meet the "least significant adder cell" in the first row recited limitation.

Applicant's claims also recite that the second adder cell in the first row receives the conditional carryout bits from the least significant adder cell and generates its two conditional carryout bits by propagating the received conditional carryout bits through a first pass gate and a second pass gate when the first input data bit (A) and the second input data bit (B) are unequal. Uya's Bit 9, Bit 14 or Bit 20 adder cells are the only adder cells that could possibly meet the "second adder cell" limitation (in the same row as the least significant adder cell) in the claims. Though not expressly disclosed, Applicant can only assume that Uya's Bit 9, Bit 14 or Bit 20 adders would be

equivalent in structure to the Bit 5 adder cell shown Figures 3 or 4. It is clear from Uya's Figure 3 that the Bit 5 adder in the row does not propagate the received carryout bits (C5) through a first pass gate and a second pass gate when the first data bit A_5 and the second data bit B_5 are unequal to generate the next carryout bits (C6). Uya, Figure 3.

The Office Action further argues that Uya's logic gates 54-55 meet Applicant's first and second pass gates. In order to be consistent with the Office Action's prior interpretation of the "least significant adder cell", Uya's C26 carryout bits are propagated based on carryout bits C19 from the adder P4 -- not based on whether two data bits A and B in a second adder are unequal, and not using pass gates. The elements in Uya described in the Office Action as meeting the specific claim elements recited in Applicant's claims simply do not meet the claimed elements as they are arranged, and the Office Action's reasoning and interpretation is inconsistent with the disclosure and teachings of Uya.

Applicant notes that the Office Action identifies carryout bits C8 as Applicant's first and second carryout bits generated from the first least significant adder cell and which are provided to the second adder cell, and also identifies the C19 carryout bits as Applicant's carryout bits received by the second adder cell. The Office Action also identifies carryout bits C25 as Applicant's carryout bits from the second adder cell that are propagated through pass gates. This is clearly erroneous.

Therefore, and in either scenario of interpretations, Uya fails to disclose each and every element as they are arranged in Applicant's claims.

As noted in the Applicant's specification, in one embodiment, the time critical data paths through the adder cells in each row are the dual carry paths. See, Specification, page 26, lines 16-20. Applicant utilizes pass gates (or switches) to decrease the delay in these paths. Uya does not disclose the recited elements/features in Applicant's independent claims (as amended).

Accordingly, the Applicant respectfully requests the Examiner withdraw the § 102(b) rejection of Claims 1-5, 8-16 and 19-31.

III. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***rmccutcheon@munckbutrus.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Munck Butrus Deposit Account No. 50-0208.

Respectfully submitted,

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Date: 12/26/2007

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Serial No.	:	09/667,164
Filed	:	September 21, 2000
For	:	M-BIT RACE DELAY ADDER AND METHOD OF OPERATION
Group No.	:	2193
Examiner	:	Chat C. Do

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